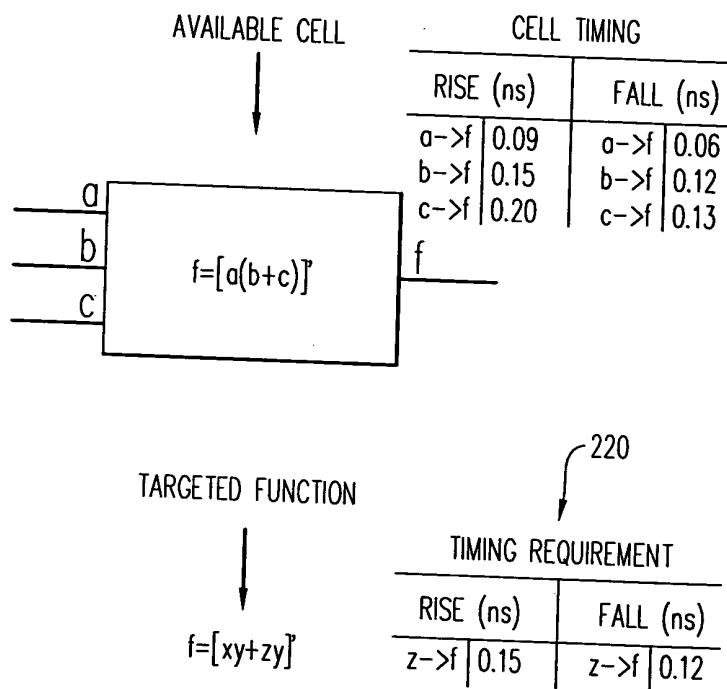
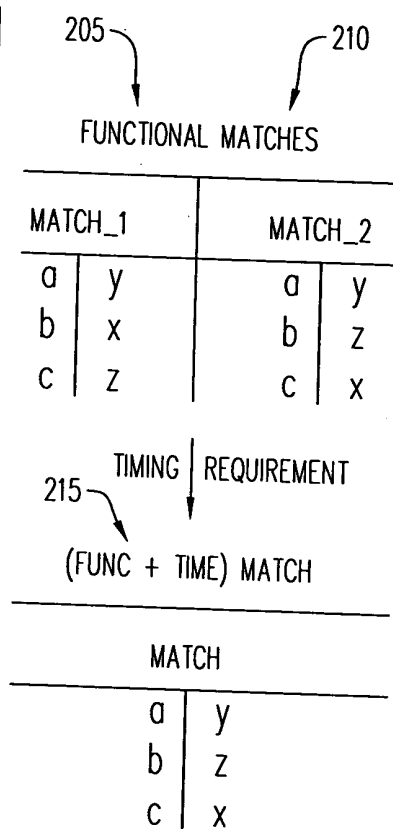




## REPLACEMENT SHEET



**FIG. 2**



**FIG. 2a**



# REPLACEMENT SHEET

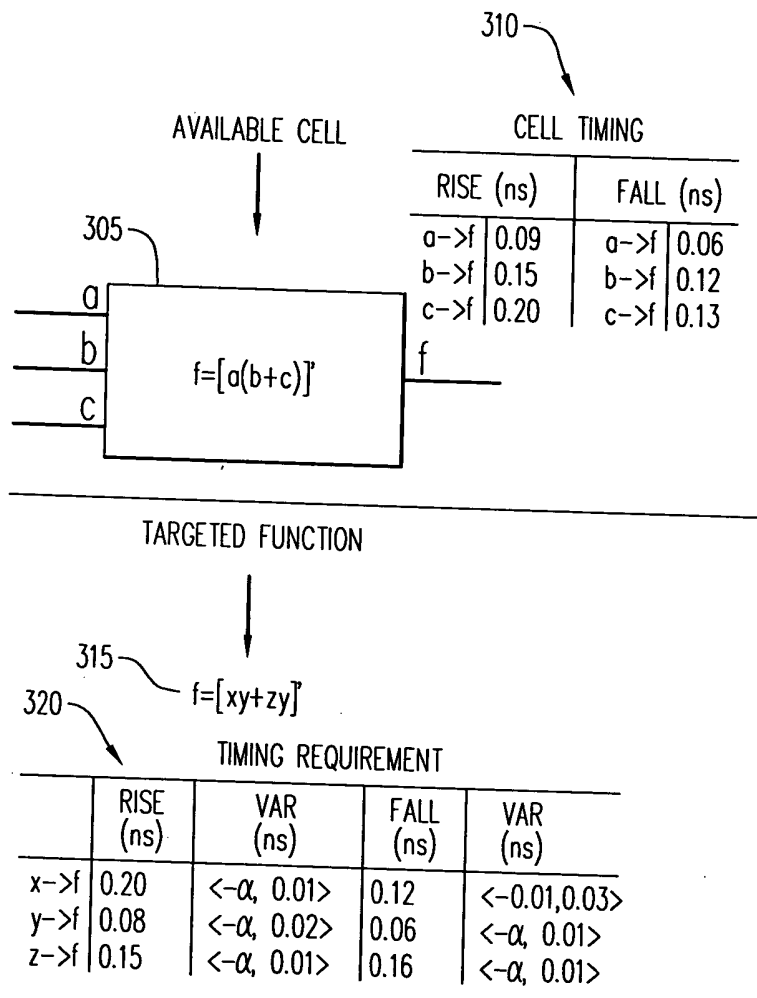


FIG. 3

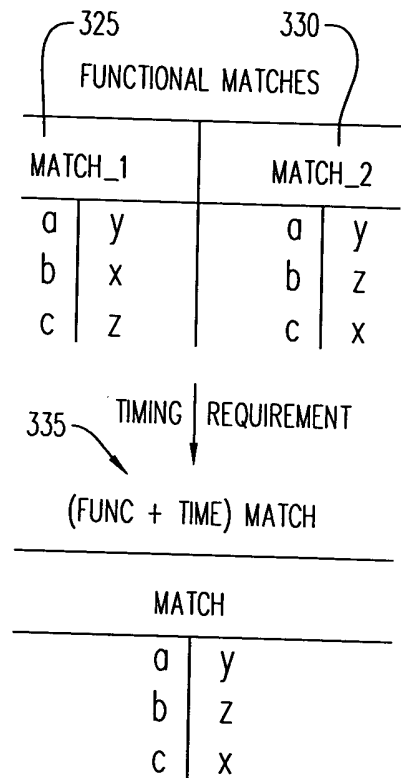
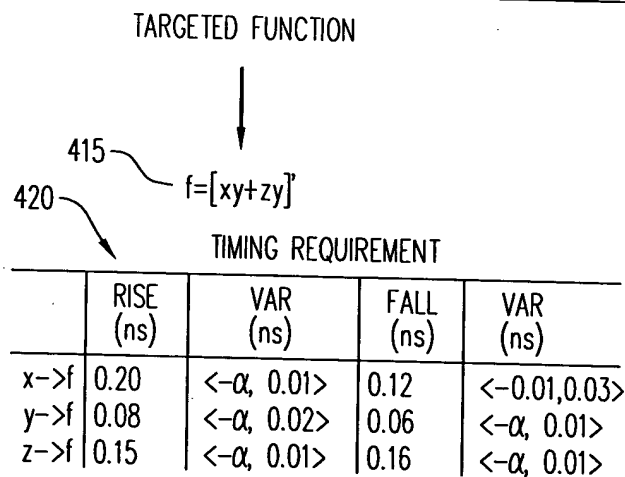
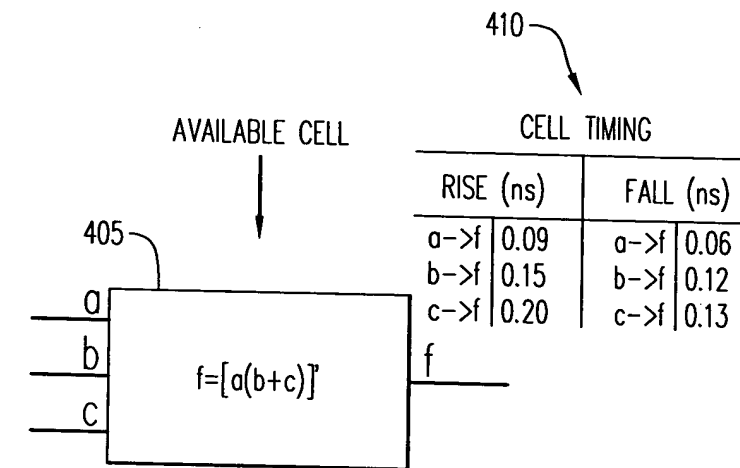


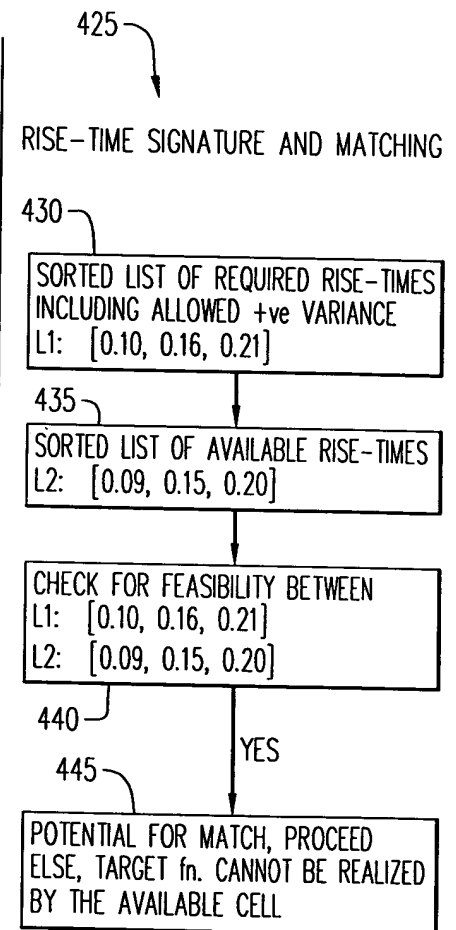
FIG. 3a



## REPLACEMENT SHEET



**FIG. 4**



**FIG. 4a**



# REPLACEMENT SHEET

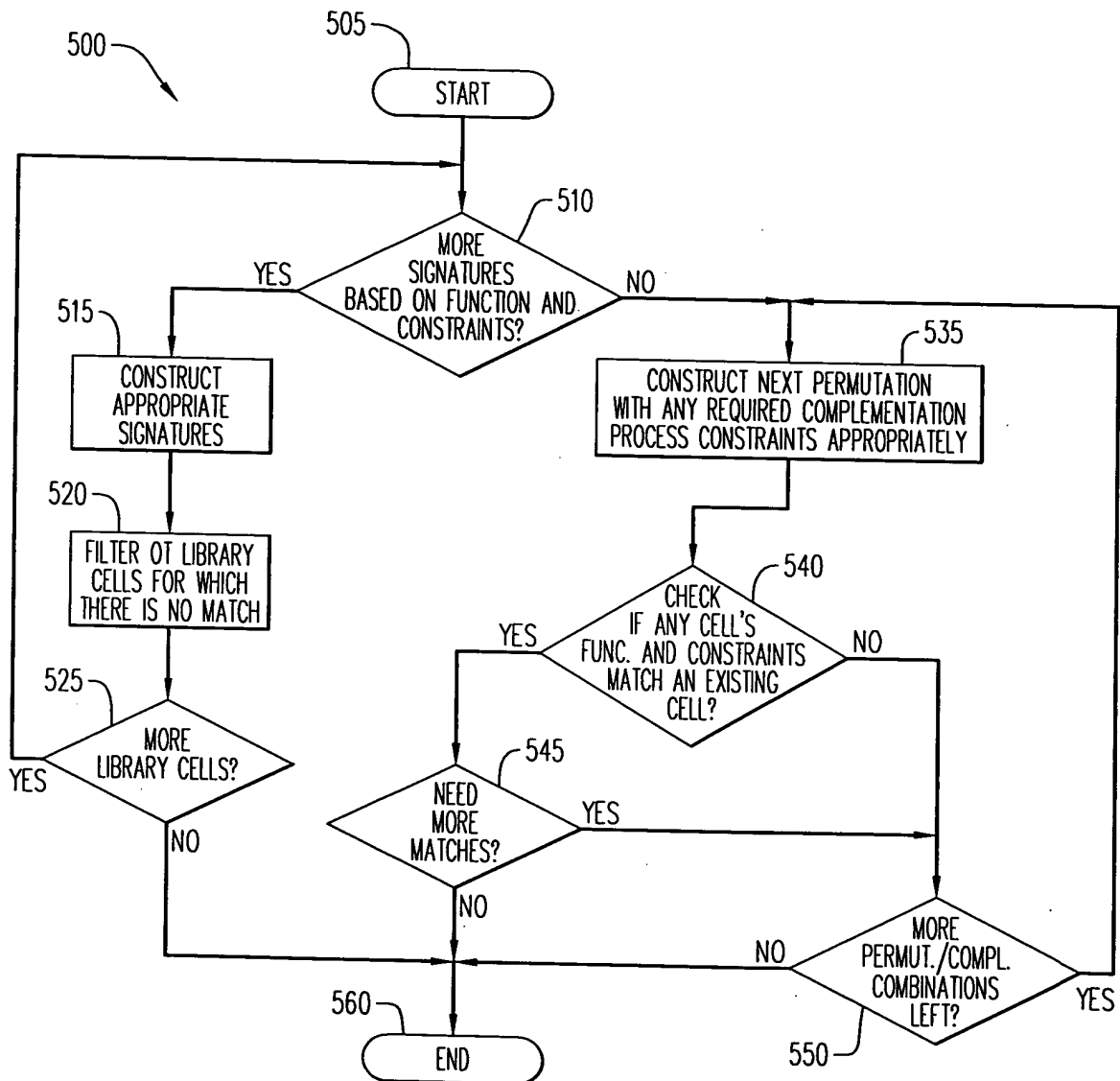
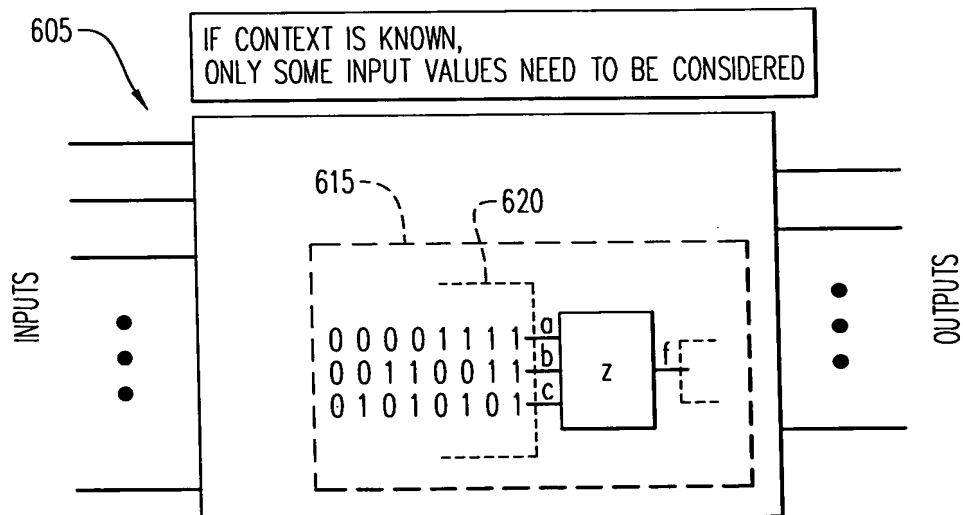


FIG. 5

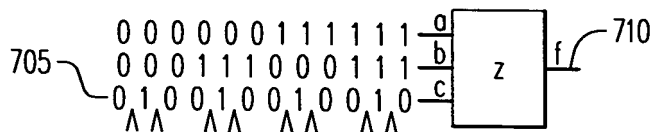


**FIG. 6**



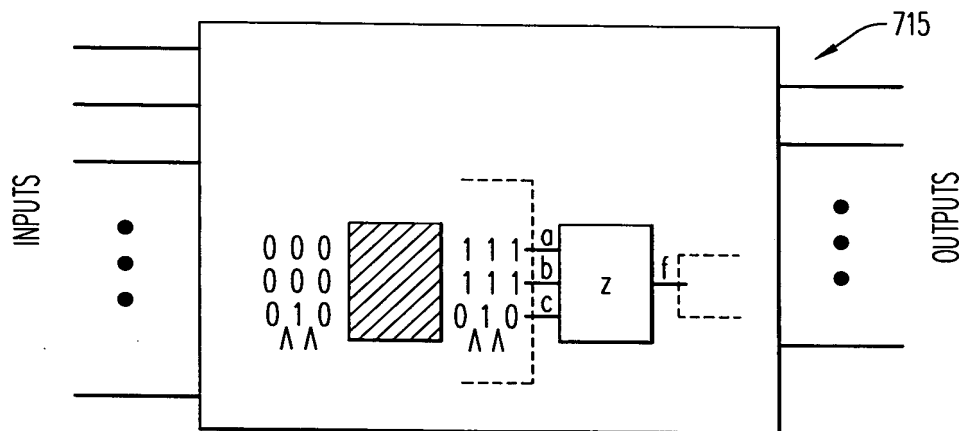
# REPLACEMENT SHEET

IF CONTEXT IS NOT KNOWN,  
TO CHARACTERIZE TIMING ON  $c \rightarrow f$   
ALL POSSIBLE 0- $\rightarrow$ 1 AND 1- $\rightarrow$ 0 TRANSITIONS  
ON C NEED TO BE CONSIDERED



IF CONTEXT IS KNOWN,  
TO CHARACTERIZE TIMING ON  $c \rightarrow f$   
ONLY SOME 0- $\rightarrow$ 1 AND 1- $\rightarrow$ 0 TRANSITIONS  
ON C NEED TO BE CONSIDERED  
(CONTEXT ELIMINATES OTHER TRANSITIONS)

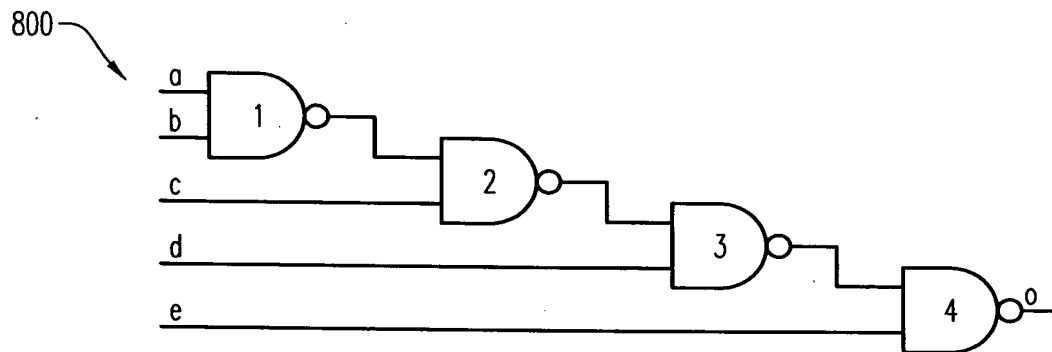
- CHARACTERIZATION IS MORE ACCURATE
- CHARACTERIZATION NEEDS LESSER RESOURCES



**FIG. 7**



## REPLACEMENT SHEET



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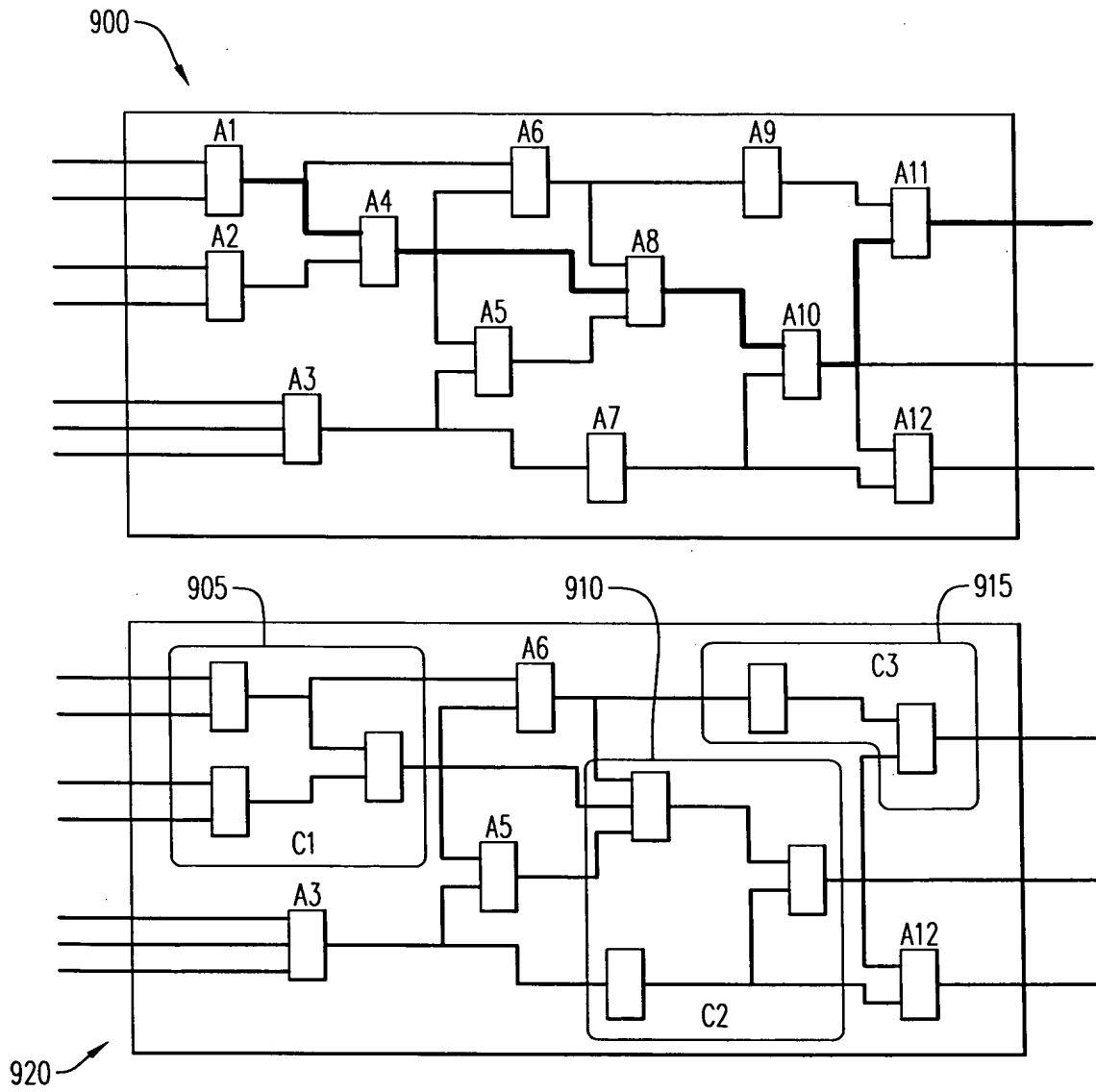
WORST PROPAGATION DELAY THROUGH THE DESIGN

DRIVE STRENGTHS AT STAGE	GATE-LEVEL TIMING (STA)	TRANSISTOR-LEVEL TIMING (SPICE)
1 2 3 4	(ns)	(ns)
0 0 0 0	0.40	0.186
1 1 1 1	0.22	0.166
2 2 2 2	0.15	0.157
4 4 4 4	0.61	0.581
0 1 2 4	0.41	0.332

**FIG. 8**



## REPLACEMENT SHEET



**FIG. 9**